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File 344:Chinese Patents Abs Aug 1985-2003/Apr
         (c) 2003 European Patent Office
File 347:JAPIO Oct 1976-2003/Jul(Updated 031105)
         (c) 2003 JPO & JAPIO
File 350:Derwent WPIX 1963-2003/UD,UM &UP=200373
         (c) 2003  Thomson Derwent
? ds

Set     Items   Description
S1      30017   (CONVERT? OR CONVERS? OR CHANG? OR MODIF? OR ADJUST? OR AL-
            TER?) AND BUS
S2       1075   S1 AND SERIAL AND PARALLEL
S3       9866   S1 AND (PARTITION? OR DIVID? OR SEPERAT? OR DIVISION? OR P-
            ART OR PARTS OR SECTION?? OR SEGMENT?? OR PORTION?? OR FRAGME-
            NT? OR PIECES OR SECTOR??)
S4       1407   ARRAY? AND (MEMORY OR BUFFER?? OR STORAGE OR STORAGE(3N)CE-
            LLS) AND PORT??
S5         14   (ONE OR SINGLE OR 1)()BUFFER?(3N)ELEMENT??
S6        627   CLOCK AND (CONTROL OR MONITOR OR DIRECT?) AND ACCESS??? AND
               (SEQUENTIAL? OR SIMULTANEOUS? OR CONCURRENT? OR COINCIDENT?)
S7       3249   (WRITE OR READ)(3N)CYCLE??
S8         21   AU=(ALOWERSSON, J? OR ROSLUND,  B? OR SUNDSTROM, P? OR ALO-
            WERSSON J? OR ROSLUND B? OR SUNDSTROM P?)
S9       9071   (PRESELECT? OR (PRE()(SELECT? OR SET OR DETERMIN? OR SELEC-
            T? OR SPECIFIED) OR PREDETERMIN? OR SPECIFIC OR SPECIFIED OR -
            SET OR PRESET))(3N)CYCLE?
S10         0   S8 AND S1
S11         0   S8 AND S6
S12         0   S8 AND S2
S13    213452   IC=H04Q?
S14         3   S8 AND S13
S15        19   S3 AND S4
S16         1   S15 AND S6
S17         1   S16 NOT S14
S18         0   S15 AND S7
S19         0   S6 AND S7 AND S5
S20        19   S6 AND S7
S21         2   S20 AND S3
S22         2   S21 NOT (S14 OR S15)
S23        80   S4 AND SERIAL? AND PARALLEL?
S24         3   S23 AND S7
S25         3   S24 NOT (S21 OR S14 OR S15)
S26         0   S23 AND S9
S27         0   S15 AND S9
S28        30   S3 AND S9
S29         0   S28 AND S4
S30         3   S28 AND BUFFER?
S31         3   S30 NOT (S24 OR S21 OR S14 OR S15)
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14/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013376005 **Image available**
WPI Acc No: 2000-547943/200050
XRPX Acc No: N00-405340
Converter for data in serial and parallel format, has twin port storage cells linked to data channels via database with buffer circuit
Patent Assignee: SWITCHCORE AB (SWIT-N)
Inventor: **ALOWERSSON J** ; **ROSLUND B** ; SUNDSTROEM P
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
SE 9804479	A	20000623	SE 984479	A	19981222	200050	B
SE 518865	C2	20021203	SE 984479	A	19981222	200304	

Priority Applications (No Type Date): SE 984479 A 19981222
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
SE 9804479	A		23	H04Q-011/04	
SE 518865	C2			H04Q-011/04	

Inventor: **ALOWERSSON J** ...

... **ROSLUND B**
International Patent Class (Main): **H04Q-011/04**

14/3,K/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013268629 **Image available**
WPI Acc No: 2000-440534/200038
XRPX Acc No: N00-328609
Buffer memory organised into cells for temporary data storage, especially for ATM exchange, maintains queues for each incoming channel and lists of idle cells
Patent Assignee: SWITCHCORE AB (SWIT-N)
Inventor: **ALOWERSSON J** ; ANDERSSON P; **ROSLUND B** ; SUNDSTROEM P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
SE 9803694	A	20000429	SE 983694	A	19981028	200038	B

Priority Applications (No Type Date): SE 983694 A 19981028
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
SE 9803694	A		11	H04L-012/56	

Inventor: **ALOWERSSON J** ...

... **ROSLUND B**
International Patent Class (Additional): **H04Q-011/04**

14/3,K/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013268623 **Image available**
WPI Acc No: 2000-440528/200038
XRPX Acc No: N00-328604

Multicasting device for e.g. ATM exchange, uses out port in exchange core to copy data packet and send it on via outgoing link and return packet with changed address to in port

Patent Assignee: SWITCHCORE AB (SWIT-N)
Inventor: **ALOWERSSON J** ; ANDERSSON P; SUNDSTROEM P
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
SE 9803583	A	20000422	SE 983583	A	19981021	200038 B
SE 514343	C2	20010212	SE 983583	A	19981021	200116
US 6625151	B1	20030923	US 99420909	A	19991020	200364

Priority Applications (No Type Date): SE 983583 A 19981021
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
SE 9803583	A		9	H04Q-011/04	
SE 514343	C2			H04Q-011/04	
US 6625151	B1			H04L-012/28	

Inventor: **ALOWERSSON J** ...
...International Patent Class (Main): **H04Q-011/04**
?

17/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008463276 **Image available**
WPI Acc No: 1990-350276/199047
Related WPI Acc No: 1993-351126
XRPX Acc No: N90-267559
Dual ported **double** buffer **video RAM - has serial** access **register which can be selected for two frame** buffers **from one** array **pixel by pixel**
Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: GUPTA S; HENDERSON R L; HILTEBEIT H R; TAMLYN R; TOMASHOT S W; WILLIAMS T; HILTEBEITEL N R; TAMLYN R J
Number of Countries: 004 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 398510	A	19901122	EP 90304325	A	19900423	199047 B
US 5065368	A	19911112	US 89352442	A	19890516	199148
EP 398510	A3	19920401	EP 90304325	A	19900423	199328
EP 398510	B1	19950208	EP 90304325	A	19900423	199510
DE 69016697	E	19950323	DE 616697	A	19900423	199517
			EP 90304325	A	19900423	

Priority Applications (No Type Date): US 89352442 A 19890516
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 398510	A				
Designated States (Regional): DE FR GB					
EP 398510	B1	E	12	G11C-008/00	
Designated States (Regional): DE FR GB					
DE 69016697	E			G11C-008/00	Based on patent EP 398510

Dual ported **double** buffer **video RAM**...

...**has serial** access **register which can be selected for two frame** buffers **from one** array **pixel by pixel**

...Abstract (Basic): The dual **ported** video **memory** consists of a dynamic random **access array** (112) with row and column decoders **accessed** by a serial **access memory** register. This register has facilities for selecting on a per pixel basis from two **alternate** frame **buffers** stored in the **array** .
...

...A double **buffer** select signal controls which half of the register is to put data onto the output **bus** on each serial **clock** signal which also increments address pointers in both halves...

...ADVANTAGE - Enables selective scan out on per pixel basis without duplication of **memory** components. (11pp Dwg.No.2A/4)
...Abstract (Equivalent): A dual- **port memory** comprising: a **memory array** (112) having a plurality of **memory** elements each of which is **accessed** at random by a row and column address input (AO-A9) to enable writing into or reading out of data at the row and column location; first and second serial **access memory** means (120, 122) for each selectively **accessing** a specified **portion** of the data of a row or column of the **memory** elements in parallel; **control** mans (102) for serially transferring out through an output **port** (SDO-SD7) the specified **portion** of data of the row or column of the **memory**

elements; and selection means (1020 for selectively coupling the first or second serial **access memory** means to the output **port** , the selection means responsive to a selection **control** signal (DBS), characterised in that the **control** means is responsive to a **clock** signal (SC) to **simultaneously** increment the addresses of the data elements which are available at the outputs of the first and second serial **access memory** means, so that, at any given time in use, output data corresponding to display pixels in one of two frame **buffers** (A, B) may be selected to be transferred to the output **port** from the first or the second serial **access memory** means on a per pixel bases...

...Abstract (Equivalent): The implementation of a serial **access memory** register facilitates the selecting from two **alternate** frame **buffers** on a per pixel basis. The frame **buffers** are each stored in a **portion** of a row in a single video Following data transfer to the serial **access memory** register, data from each of the two frame **buffers** is RAM. available. A double **buffer** select signal controls the selection of which half of the serial **access memory** register will put data on the output **bus** for each serial **clock** signal. The serial **clock** increments the address pinters in both halves of the serial **access memory port simultaneously** .

(

...Title Terms: **PORT** ;

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22/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009914308 **Image available**
WPI Acc No: 1994-182018/199422
XRPX Acc No: N94-143722
Hard drive accelerating system - decomposes CPU input-output command to read or write hard disk drive into two separate tasks that can be executed concurrently **, and uses read buffer and write buffer to link two tasks**
Patent Assignee: EFAR MICROSYSTEMS INC (EFAR-N)
Inventor: CHANG I; HSU R; CHANG Y; SHEU J
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
TW 222694	A	19940421	TW 93107625	A	19930917	199422	B
US 5594926	A	19970114	US 9393373	A	19930719	199709	

Priority Applications (No Type Date): US 9393373 A 19930719
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
TW 222694	A		6	G06F-012/00	
US 5594926	A		20	G06F-013/00	

... **to read or write hard disk drive into two separate tasks that can be executed** concurrently **, and uses read buffer and write buffer to link two tasks**

...Abstract (Basic): or write a hard disk drive (18) into two separate tasks that can be executed **concurrently** . A read buffer (40) and a write buffer (42) are used to link the two...

...A state machine (48) generates consecutive I-O **read cycles** to fetch data from the hard drive to the read buffer while the CPU executes I-O commands to retrieve data from the read buffer. A programmable hardware register (49) **adjusts** the hard disk I-O cycle time to achieve maximum compatibility with different hard drive...

...Abstract (Equivalent): drive, a system memory, and a central processing unit (''CPU'') for generating input-output (''IO'') **read** /memory **write cycles** to transfer data from the hard drive to the system memory and for generating memory **read** /IO **write cycles** to transfer data from the system memory to the hard drive, the hard drive being **divided** into **sectors** and having a hard-drive data register, the CPU and system memory being coupled to a first **bus** , the hard drive being coupled to a second **bus** that operates at a lower **clock** rate than the first **bus** , the accelerating system comprising the following elements for decomposing disk **access** operation for each of read and write into at least two tasks which can be executed **concurrently** :
...

...a **control** and state machine that comprises...

...the read buffer from the hard drive since the accelerating system began to read a **sector** of the hard drive...

...address register for pointing to a unit of the read buffer for the CPU to **access** ;
(...

...the hard drive, determining when to start, suspend, resume, and end fetching data from a **sector** of the hard drive, generating hard drive

read cycles to **read** data from the hard drive, causing data to be transferred from the hard drive to the read buffer during a hard drive **read cycle concurrently** while data is being transferred from the read buffer to the system memory during a prior IO **read** /memory **write cycle** , generating hard drive **write cycles** to **write** data to the hard drive, and causing data to be transferred from the write buffer to the hard drive during a hard drive **write cycle concurrently** while data is being transferred from the system memory to the write buffer during a subsequent memory **read** /IO **write cycle** .

...Title Terms: **CONCURRENT** ;

22/3,K/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008285884 **Image available**
WPI Acc No: 1990-172885/199023
Related WPI Acc No: 1995-053877; 1995-053878; 1997-300512; 1997-300513; 1997-300514; 1997-300515; 1997-473480; 1997-473481
XRPX Acc No: N90-134457
Dynamic video random access **memory - has internal circuitry for performing either image mode or vector mode addressing of line of stored video information**
Patent Assignee: MATSUSHITA ELEC IND CO LTD (MATU); MATSUSHITA DENKI SANGYO KK (MATU); MATSUSHITA ELECTRIC IND CO LTD (MATU); SOLBOURNE COMPUTER INC (SOLB-N)
Inventor: HARLIN R E; HERRINGTON R A
Number of Countries: 005 Number of Patents: 013
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 371488	A	19900606	EP 89122020	A	19891129	199023	B
US 5142637	A	19920825	US 88277637	A	19881129	199237	
US 5148523	A	19920915	US 88278333	A	19881129	199240	
US 5148524	A	19920915	US 88277687	A	19881129	199240	
EP 371488	A3	19920812	EP 89122020	A	19891129	199336	
JP 7271657	A	19951020	JP 89310233	A	19891129	199551	
			JP 9551626	A	19891129		
JP 7271970	A	19951020	JP 89310233	A	19891129	199551	
			JP 9551624	A	19891129		
JP 7287978	A	19951031	JP 89310233	A	19891129	199601	
			JP 9551625	A	19891129		
JP 7325752	A	19951212	JP 9551626	A	19891129	199607	
			JP 9576875	A	19891129		
EP 371488	B1	19960131	EP 89122020	A	19891129	199609	
JP 8007565	A	19960112	JP 9551626	A	19891129	199611	
			JP 9576899	A	19891129		
DE 68925569	E	19960314	DE 625569	A	19891129	199616	
			EP 89122020	A	19891129		
US 35680	E	19971202	US 88277687	A	19881129	199803	
			US 94306180	A	19940914		
			US 95574858	A	19951219		

Priority Applications (No Type Date): US 88278333 A 19881129; US 88277637 A 19881129; US 88277687 A 19881129; US 94306180 A 19940914; US 95574858 A 19951219
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 371488	A				

Designated States (Regional): DE FR GB

US 5142637	A	23	G06F-003/153	
US 5148523	A	25	G09G-001/02	
US 5148524	A	25	G06F-012/02	
JP 7271657	A	27	G06F-012/00	Div ex application JP 89310233
JP 7271970	A	25	G06T-001/60	Div ex application JP 89310233
JP 7287978	A	26	G11C-011/401	Div ex application JP 89310233
JP 7325752	A	24	G06F-012/02	Div ex application JP 9551626
EP 371488	B1 E	32	G09G-001/16	

Designated States (Regional): DE FR GB

JP 8007565	A	25	G11C-011/401	Div ex application JP 9551626
DE 68925569	E		G09G-001/16	Based on patent EP 371488
US 35680	E	28	G06F-012/02	Cont of application US 94306180 Reissue of patent US 5148524

Dynamic video random access **memory**...

...Abstract (Basic): on the addressed line of stored video information which includes the write masking circuitry for **modifying portions** of the line between selected START and STOP bit locations...

...A single **clock** is employed to operate the random port to perform refresh, memory address, and to **control** the internal circuitry for inputting data and addresses and for outputting data as well as **modifying** information in the memory circuit chip...

...Abstract (Equivalent): use in raster scan graphic applications in the form of a high density video random **access** memory, placed on a single integrated circuit chip so as to perform on-chip **modifications** of the stored video information, said dual ported dynamic memory device being connected to a random **bus** (90, 100, 140), said architecture being characterized by a memory (1300) for storing video information...

...column in said page, and further by an address means (1320) connected to said random **bus** for receiving an address for specifying a horizontal or vertical vector in a page of said memory to be **modified** , said address comprising: (a) a first plurality of bits for defining a pge row of...

...said page row and said page column, a data means (1340) connected to said random **bus** for receiving **modifying** data used to **modify** video information stored in said memory, and a write mask means (1336) connected to said memory for allowing to **modify** video information stored at said address in said memory in a specified range of bit locations; and a **control** means (1354, 1360, 1366) connected to said random **bus** , said memory, said address means, and said data means for **modifying** said video information stored at said address in said memory in accordance with said **modifying** data in said specified range of bit locations, on said single integrated circuit chip...

...Abstract (Equivalent): column locations respectively. The address of a vector in a page of memory to be **modified** is received (1360). The address comprises several bits defining the page row, column and the addressed vector in page. A data register (1340) connected to the **bus** , receives the source data. The controller (1366, 1360, 1354, 1336) is connected to the memory...

...The method involves the step of receiving on the integrated circuit chip from the **bus** during an interval of the write **portion** of the **read / write cycle** , the address for a line of stored information in the dynamic video random **access** memory to be **modified** . The drawing rule contg. a logical operation and the START and STOP bit locations for

modifying the line of stored information between identified beginning and ending bot locations are also received...

...logically combined with the line of stored information during a second interval of the write **portion** of the **read / write cycle** . The dynamic video random **access** memory is addressed during this second interval with the received address and the line of stored information is read out. During a third time interval of the write **portion** , the read out line of stored information is logically combined on chip with the source data based upon the received drawing rule. The dynamic video random **access** memory is written to, during a fourth time interval of the write **portion** with the logically combined line of information between the START and STOP bit locations so as to fully **modify** the addressed line of stored information during the **read / write cycle** . USE/ADVANTAGE - For on chip line **modification** of dynamic video RAM with CAD/CAM systems. Masking circuit responds to address and drawing rule **simultaneously** so executes each address cycle...

...The architecture for a single chip dynamic video random **access** memory uses a single **clock** to operate the random port to perform refresh, memory address, and to **control** the internal circuitry. The **clock** governs the input and output of data as well as **modifying** information in the memory circuit chip. The memory chip has internal circuitry for performing drawing...

...line of stored video information in the RAM and further has write masking circuitry for **modifying** selected **portions** of the line of stored video information between selected start and stop bit locations within...

...raster scan graphic applications partic. high density dynamic VRAM on single IC with single random **part clock** . Min. number of signal paths to/from chip and faster operation...

...Title Terms: **ACCESS** ;

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25/3,K/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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03658194 **Image available**
MULTI- **PORT** VIDEO **MEMORY**

PUB. NO.: 04-023294 [JP 4023294 A]
PUBLISHED: January 27, 1992 (19920127)
INVENTOR(s): OI YASUSHI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-129564 [JP 90129564]
FILED: May 18, 1990 (19900518)
JOURNAL: Section: P, Section No. 1347, Vol. 16, No. 186, Pg. 147, May 07, 1992 (19920507)

MULTI- **PORT** VIDEO **MEMORY**
...JAPIO CLASS: **Memory** Units); 42.2 (ELECTRONICS

ABSTRACT
... plotting and moving image input by performing control for the priority of a random data **port** and switching of priority at a **serial** random data **port** when write on the same row occurs from a **serial** data **port** and a random data **port** .

...

...CONSTITUTION: When a write operation from the random data **port** is executed in **parallel** with a **serial** external **write cycle** , and after that, a **serial** internal **write cycle** is executed, a multiplexer selects the output 129 of a **serial** register 106 updated by the **serial** external **write cycle** or that of a random write register that is the information of the row updated...

...dirty bit register. The write of a random access side can be stored in a **memory** cell **array** 109 preferentially to that of a **serial** access side.

25/3,K/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2003 Thomson Derwent. All rts. reserv.

008820781 **Image available**
WPI Acc No: 1991-324794/199144
XRPX Acc No: N91-249034
Address register processor system for multiple- port memory **- has controller connected to data queue into** memory array **for timing** read - write cycles **, and data output receiver**
Patent Assignee: TEXAS MED INSTR INC (TEXA-N)
Inventor: BROOKS T K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5058051	A	19911015	US 88225742	A	19880729	199144	B

Priority Applications (No Type Date): US 88225742 A 19880729

Address register processor system for multiple- port memory - ...

...**has controller connected to data queue into** memory array **for timing** read - write cycles , **and data output receiver**

...Abstract (Basic): digital information, a data queue connected to the data input by a data bus, a **memory array** interactive with the data queue, a **memory** controller connected to the data queue into the **memory array** for timing the **read / write** signal **cycles** of the **memory array** in response to the state of the data queue, and a data output receiver connected...

...The data queue performs **serial** -to- **parallel** conversion of the input data from the input data source. The data queue also performs 1parallel -to- **serial** conversion on the output data to the data output receiver. The input data source comprises a large contiguous lock of **memory** data connected to the data queue by a set of **ports** . Each of the **ports** is independent of any of the other **ports** . The data queue is a loadable shift register having a set of data paths extending from the input data source, the **memory** controller, and the data output receiver...

...USE/ADVANTAGE - multiple **port memory** system for multi-processing or distributed processing. (14pp Dwg.No.1/5)
...Title Terms: **PORT** ;

25/3,K/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008300470 **Image available**
WPI Acc No: 1990-187471/199025
Related WPI Acc No: 1984-115650; 1990-158055; 1990-173292
XRPX Acc No: N90-145787
Electronic system for video display - has memory **with** serial **and** parallel **data accessing** ports **for supplying bit-mapped display**
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: HUGHES J M; LAFFITTE D S; MCDONOUGH K C
Number of Countries: 004 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 374127	A	19900620	EP 90100606	A	19830914	199025	B
EP 374127	B1	19950412	EP 83109060	A	19830914	199519	
			EP 90100606	A	19830914		
DE 3382784	G	19950518	DE 3382784	A	19830914	199525	
			EP 90100606	A	19830914		

Priority Applications (No Type Date): US 82427236 A 19820929
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 374127	A				
Designated States (Regional): DE FR GB NL					
EP 374127	B1	E	20	G09G-001/16	Related to application EP 83109060
Designated States (Regional): DE FR GB NL					
DE 3382784	G			G09G-001/16	Based on patent EP 374127

... **has** memory **with** serial **and** parallel **data accessing** ports **for supplying bit-mapped display**

...Abstract (Basic): A shift register (20) is provided in the **memory** (10) with two identical halves of the register provided, one at either side

of the **memory** . The register is loaded from column lines of the **memory** **array** for a **read** **cycle** or loads the column lines for a **write** **cycle** using transfer gates at either side of the **array** . Data, from a source of **serial** data, are written into **memory** locations through the **serial** shift register and are able to be manipulated by the microprocessor (8) through the **parallel** access part...

...The display (1) is then able to produce a video image corresponding to the **serial** data input in response to the data read from the **memory** through the shift register...

...USE/ADVANTAGE - In microcomputer using magnetic disc for bulk **storage** , allowing the contents of **memory** **array** to be read out to disc store through one part whilst data are being written into **memory** through other part. In interactive home TV system for games, education or catalogue ordering. (20pp...

...Abstract (Equivalent): an image; a source (105) of data from which an image can be formed; a **memory** (5) arranged for both **parallel** and **serial** access; said **parallel** access being arranged for access by a processor (8) such that stored data may be...

...such that processed data may be stored; characterised in that said source (105) applies data **serially** to said **memory** (5) and said display (1) receives data **serially** from said **memory** (5), said **serial** access being by virtue of a **serial** register (20) arrangement of said **memory** (5) such that said data from said source (105) may be stored into said **memory** (5) and such that stored data may be read therefrom to enable the display (1...

...Title Terms: **MEMORY** ;

?

31/3,K/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06867073 **Image available**
ISOCHRONOUS PACKET TRANSFER METHOD, RECORDING MEDIUM FOR TRANSFER CONTROL PROGRAM, BRIDGE AND PACKET TRANSFER CONTROL LSI

PUB. NO.: 2001-094576 [JP 2001094576 A]
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INVENTOR(s): DOMON WATARU
APPLICANT(s): NEC CORP
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ABSTRACT
...TO BE SOLVED: To provide an isochronous packet transfer method which can decrease the transmitting **buffer** size needed for isochronous packet transfer and give certain delay to isochronous packets even if...

...transmission of a cycle start packet is delayed.

SOLUTION: An isochronous packet received from a **bus** 40 is inputted to a delay **part** 111, delayed according to delay information 109, and sent to a **bus** 41. Cycle identification information generation **part** 103 and 104 outputs **pieces** 101 and 102 of cycle identification information which **change** in the timing of the transmission of the cycle start packet to the buses 40 and 41. Reference cycle identification information generation **parts** 107 and 108 sample the **pieces** 101 and 102 of **cycle** identification information in **specific** timing and outputs **pieces** 105 and 106 of reference cycle identification information. A delay information generation **part** 110 adds fixed delay to the difference between the numbers of elapsed cycles by the buses from the mentioned specific timing according to the **pieces** 101 and 102 of cycle identification information and **pieces** 105 and 106 of reference cycle identification information to generate delay information 109.

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31/3,K/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

03827074 **Image available**
DUAL PORT RAM

PUB. NO.: 04-192174 [JP 4192174 A]
PUBLISHED: July 10, 1992 (19920710)
INVENTOR(s): FUKUDA HIROYUKI
OGAWA TOSHIYUKI
APPLICANT(s): MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-326966 [JP 90326966]
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JOURNAL: Section: P, Section No. 1444, Vol. 16, No. 520, Pg. 125, October 26, 1992 (19921026)

ABSTRACT
PURPOSE: To execute cross scroll of a screen display by a mere **change** of

a start address by previously setting a pit length and jumping to the start address of a separate **divided** data register after the completion of the reading out bit length at the time of...

...CONSTITUTION: The bit length is **set** by a CBR **cycle** before a split transfer cycle and thereafter, the addresses of N lines and K rows...

... the N lines appear in the bit lines after sense amplification. Simultaneously a column address **buffer** 12 and a data register 5 are connected by receiving the signal of .phi. from...

...The address is then jumped to the K address put into the counter of the **divided** upper or lower register 5. Finally, internal serial **bus** data are outputted.

31/3,K/3 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007580278
WPI Acc No: 1988-214210/198831
Data input circuit for data processing equipment - has input data latched asynchronously of read request signal produced by central processing unit, by using pulse generated by timing circuit
Patent Assignee: NEC CORP (NIDE)
Inventor: AKASHI M
Number of Countries: 005 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 276794	A	19880803	EP 88101025	A	19880125	198831	B
US 4999807	A	19910312	US 88148309	A	19880125	199113	
EP 276794	B1	19960529	EP 88101025	A	19880125	199626	
DE 3855314	G	19960704	DE 3855314	A	19880125	199632	
			EP 88101025	A	19880125		

Priority Applications (No Type Date): JP 8714944 A 19870125
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 276794	A	E	11		
EP 276794	B1	E	11	G06F-013/42	
Designated States (Regional): DE FR GB IT					
DE 3855314	G			G06F-013/42	Based on patent EP 276794

...Abstract (Basic): A level **conversion** circuit at input terminals (1-0..1-7) of the input circuit has a resistor...

...take a potential level intermediate that of logic one and logic zero. Consequently, the level **conversion** circuit operates for **converting** that intermediate level into the logic level required by the CPV. When the CPV generates address information which selects the comparator port (100), a **bus** **buffer** (7) is activated to couple a set of output nodes of the latch circuit (6) to the data **bus** .
...

...decoder and flip-flop are operative in response to address data output on the address **bus** (9) for accessing the input circuit, to prevent the clock signal from being supplied to a **divider** which supplies the operating control signal and latch enable signal. This prevents the latch enable

...Abstract (Equivalent): a timing circuit (10) generating said latch pulse, at least one output terminal (8), a **buffer** circuit (7) receiving a read request signal (RE) and coupling said output node of said...

...circuit (10) generate said operating control signal which takes said first and second logic levels **alternatively** in a **predetermined cycle** , generates said latch pulse for constant period of time at the end of a period...

...said second logic level of said operating control signal such that said read request signal **changes** form said active level to an inactive level before said latch pulse is generated...

...Abstract (Equivalent): the latch pulse. The data latched in the latch circuit is transferred to a data **bus** in response to the read request signal...

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